CHECKPOINT COMPUTER SYSTEM UTILIZING A FIFO BUFFER TO RE-SYNCHRONIZE AND RECOVER THE SYSTEM ON THE DETECTION OF AN ERROR

ABSTRACT

A fault-tolerant computer system having an application memory organized as a plurality of cache lines, each cache line being identified by an address in the memory. A FIFO buffer stores a plurality of such cache lines. The system includes at least one CPU for executing instructions stored in the application memory. A checkpoint controller defines a series of repeating checkpoint cycles. The application memory and FIFO buffer are operated under the control of a memory controller. The checkpoint controller also has access to a plurality of registers in the CPU that define the state of that CPU at a point in each checkpoint cycle that is controllable by the controller. When the memory controller receives a cache line from the CPU in response to a write command specifying an address A in the application memory at which the cache line is to be stored, a copy of the cache line as stored in the application memory at A is copied into the FIFO buffer upon receiving the first write command specifying A after the start of the current checkpoint cycle. The cache line received in the write command is then used to overwrite the contents of address A in the application memory. At a predetermined point in each checkpoint cycle, the checkpoint controller causes the CPU to write back to the memory all dirty cache lines; and to store its internal registers defining the state of the CPU in the state memory. The checkpoint controller empties the contents of the FIFO buffer at the end of each checkpoint cycle if no error has been detected by the end of the checkpoint phase of the cycle. If an error is detected, the contents of the FIFO buffer are read back into the application memory, and the contents of the state memory are read back into the CPU. The system is then restarted after completing any hardware configuration needed for the restart.